ABSTRACT OF THE DISCLOSURE

A semiconductor component configured for wafer-level testing includes a semiconductor die having at least one die contact electrically exposed for coupling with a redistribution circuit that electrically couples at least one die contact to an extended contact such as a bumped contact. The component further includes a bus conductor that traverses at least a portion of the die and electrically mates with corresponding bus conductors on other similarly prepared components on the wafer. Functional and nonfunctional dice are identified on the wafer and the nonfunctional dice are isolated from the wafer-level testing grid. Following test, dice may be subsequently tested or moved to singulation wherein the die-to-die interconnection is interrupted, allowing wafer-level tested components to be conventionally assembled. A wafer may be retrofit with the wafer-level redistribution circuit for facilitating wafer-level testing without requiring customization of test fixtures or software for avoiding testing of nonfunctional dice.